CURRICULUM VITAE

J. Robert Heath
Department of Electrical and Computer Engineering
University of Kentucky
Lexington, KY 40506

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PERSONAL

Office Address: Department of Electrical and Computer Engineering
453 F. Paul Anderson Tower
University of Kentucky
Lexington, KY 40506
Phone: (859) 257-3124, Email: heath@engr.uky.edu
Fax: (859) 257-3092

Marital Status: Married With Children

Citizenship: USA

EDUCATION

Ph.D., Electrical Engineering (Computer Engineering Emphasis), Auburn University, 1973.
M.S., Electrical Engineering (Computer Engineering and Discrete Control System Emphasis), Auburn University, 1969.
B.S., Electrical Engineering, Auburn University, 1967.

PROFESSIONAL EMPLOYMENT AND AFFILIATIONS

Director of Undergraduate Studies for Computer Engineering Program, University of Kentucky, July, 2005-Present.
Visiting Scholar, School of Electrical and Computer Engineering, Purdue University, January, 2002-May, 2002
Research Associate, The Laboratory for Advanced Networking, University of Kentucky, 2001-Present
Director, Computer Architecture Research Laboratory, University of Kentucky, 2000 – Present
Research Associate, Army Research Laboratory, Ft. Monmouth, NJ, Summer, 1995
Associate Vice President for Information Systems Planning and Policy and Director of the Computing Center, University of Kentucky, 1984-1987.
Director of University Computing, University of Kentucky, 1982-1984.
Associate Professor, University of Kentucky, 1981-Present
Assistant Professor, University of Kentucky, 1978-1980
Adjunct Assistant Professor, Auburn University, 1974-1978
Assistant Professor, University of South Carolina, 1973

Instructor, Auburn University, 1972
Engineer, U.S. Army Missile Command, Huntsville, AL, Summer, 1971

PROFESSIONAL ACTIVITIES

Alabama Society of Professional Engineers (Reg. No. 11835)
Association for Computing Machinery (ACM)
IEEE, Senior Member, Professional Group on Computers , Professional Group on Communications and Professional Group on Industry Applications
Publication Review (IEEE and International Journals, International and Regional Conferences)
Conference Participation (Program Committee and Session Chairs-IEEE International and Regional Conferences)
The International Society for Optical Engineering (SPIE)
CAUSE
EDUCOM

AWARDS AND HONORS

Eta Kappa Nu
Sigma Alpha Epsilon, Auburn University Chapter Scholar of the Year Award, 1967
Sigma Xi (Full Member)
Tau Beta Pi
AAES Who's Who in Engineering

COURSES TAUGHT

1. FORTRAN And BASIC Programming (Fr. Level)
2. Electrical Engineering Circuits (Soph. Level)
3. Design of Logic Circuits (Soph. Level)
4. Computer Organization And Design (Jr. Level)
5. Electrical Engineering Analysis And Transform Methods (Sr. Level)
6. Electronics (Sr. Level)
7. Microprocessors (Sr. Level)
8. Advanced Logical Design (Sr. and Grad. Level)
9. Switching Theory (Grad. Level)
10. Automata And Finite-State Machine Theory (Grad. Level)
11. Compiler Design (Grad. Level)
12. Digital Computer Structure And Architecture (Grad. Level)
13. Advanced Computer Architecture Design (Sr. and Grad. Level)
14. Hardware Description Languages (Verilog, VHDL, SystemVerilog) and Programmable Logic (Sr. and Grad. Level)
15. Computer Design and Implementation (Sr. Level)

AREAS OF RESEARCH SPECIALIZATION

Digital Systems Theory, Modeling, Analysis, Design, Simulation, Synthesis/Implementation, and Testing

Computer Engineering (Application Specific Computer Architecture Development and Validation - Uniprocessor, Parallel, Distributed, Reconfigurable, Dynamic, Data-Driven and Hybrid Systems; Computer Aided Design and Synthesis; Formal Specification and Validation/Verification of Digital Systems; Computer Performance Evaluation)

Digital Signal Processing, Image Processing, Communications Processing and Control Systems

GRANTS AND CONTRACTS

1.

Principle Investigator:	Instruction/Research CAD Software Grant
Title:	Digital System Synthesis, Implementation and Simulation Computer Aided Design Software for Instructional and Research Laboratory Use: Site 132480, Support Quotation 351303R00
Funding Agency:	Mentor Graphics Corporation Higher Education Program Wilsonville, OR 97070 (Contact: Shari Benedict)
Funding Level:	$47,500.00 – (95 Copies ModelSim SE and Other CAD Software for UK Microlabs and ECE Dept. Inst. And Res. Labs)
Duration:	November 1, 2010 – October 31, 2011

2.

Principle Investigator:	Contract/Account No. 3046947100
Title:	Systematic Approach to SOC Evaluation and Verification
Funding Agency:	Lexmark International, Inc. 740 W. New Circle Rd. Lexington, KY 40550
Funding Level:	$107,539.10
Duration:	October 1, 2005 – May 31, 2010

3.

Principle Investigator:	Instruction/Research CAD Software Grant
Title:	Digital System Synthesis, Implementation and Simulation Computer Aided Design Software for Instructional and Research Laboratory Use: Site 132480, Support Quotation 267745R00
Funding Agency:	Mentor Graphics Corporation Higher Education Program Wilsonville, OR 97070 (Contact: Shari Benedict)
Funding Level:	$45,500.00 – (91 Copies ModelSim SE 6.4a CAD Software)
Duration:	September 30, 2008 – December 31, 2010

4.

Co- Investigator:	Contract/Account No. 3048082200
Title:	Anti-Sniper Infrared Targeting Systems (ASITS) Phase IIIa
Funding Agency:	M2 Technologies Inc. P.O. Box 438 Harrodsburg, KY 40330
Funding Level:	$125,865.00
Duration:	January 1, 2007 – December 31, 2008

5.

Principle Investigator:	Instruction/Research CAD Software Grant
Title:	Digital System Synthesis, Implementation and Simulation Computer Aided Design Software for Instructional and Research Laboratory Use: Site 132480, Support Quotation 216003R00
Funding Agency:	Mentor Graphics Corporation Higher Education Program Wilsonville, OR 97070 (Contact: Debbie Galyon)
Funding Level:	$52,689.00 – (91 Copies ModelSim SE 6.1a CAD Software)
Duration:	August 3, 2007 – September 30, 2008

6.

Principle Investigator:	Contract/Account No. 5-32320
Title:	Advanced Debugging Techniques and Procedures for Real-Time JPEG/DCT ASIC Implementation
Funding Agency:	Lexmark International, Inc. 740 W. New Circle Rd. Lexington, KY 40508
Funding Level:	$20,313.00
Duration:	January 1, 2004 – December 17, 2004

7.

Principle Investigator:	Contract/Account No. 2-00488
Title:	Advanced Debugging Techniques and Procedures for Real-Time JPEG/DCT ASIC Implementation
Funding Agency:	Lexmark International, Inc. 740 W. New Circle Rd. Lexington, KY 40508
Funding Level:	$9,694.00
Duration:	August 25, 2003 – December 26, 2003

8.

Principle Investigator:	Instruction/Research CAD Software Grant
Title:	Digital System Synthesis, Simulation, and Implementation Computer Aided Design Software for Instructional and Research Laboratory Use: FEIN #77-0188631 (XUP-17248, XUP-24068, and XUP-24069)
Funding Agency:	Xilinx University Program, San Jose, CA 95124
Funding Level:	$14,343.00 – XUP-17248 $13,801.00 – XUP-24068, XUP-24069
Duration:	September 30, 2002 and November 24, 2003

9.

Principle Investigator:	Contract No. 5-37947
Title:	Development, Prototyping, and Experimental Evaluation of a High Performance Processor Architecture for 2-Dimensional 5×5 Convolution of Full Page 600 DPI Images
Funding Agency:	Lexmark International, Inc. 740 W. New Circle Rd. Lexington, KY 40508
Funding Level:	$25,000.
Duration:	May 7, 2001-May 6, 2002

10.

Principle Investigator:	Instruction/Research CAD Hardware Grant
Title:	Field Programmable Gate Array Prototyping Boards for Instructional and Research Laboratory Use: XUP 6889 and 7056
Funding Agency:	Xilinx University Program San Jose, CA 95124
Funding Level:	$1372.00
Duration:	January 25, 2001

11.

Co-Principle Investigator:	Contract No. 461409
Title:	Testability Analyses of FPGAs
Funding Agency:	Cypress Semiconductor Co. San Jose, CA
Funding Level:	$96,484.
Duration:	October 1, 1997-December 31, 2000

12.

Principal Investigator:	Instruction/Research CAD Software/ Hardware Grant
Title:	Xilinx CAD Software/Hardware for Computer Design/Synthesis/Testing: XUP-4833 and XUP- 4834
Funding Agency:	Xilinx University Program 2100 Logic Dr. San Jose, CA 95124
Funding Level:	$33,076.
Date:	July 9, 1999

13.

Co-Principle Investigator:	Contract No.462364
Title:	On-Line FPGA Testing and Reconfiguration
Funding Agency:	Lucent Technologies Engineering Research Center
Funding Level:	$46,690
Duration:	June 30, 2000-May 24, 2001

14.

Principle Investigator:	Contract No. 463424
Title:	CPLD Based Embedded Logic Analyzer
Funding Agency:	Cypress Semiconductor Co.
Funding Level:	$35,000
Duration:	June 26, 2000-May 5, 2001

15.

Principal Investigator:	CAD Software Grant
Title:	ORCA Foundry 9.2 Synthesis Software
Funding Agency:	Lucent Technologies, Inc. Allentown, PA
Funding Level:	$9,000.
Date:	May, 1998

16.

Principle Investigator:	Computer Hardware Grant
Title:	MACH V CPLD and K6 Processor Chips
Funding Agency:	Vantis/AMD Corporation TX
Funding Level:	$1,182.
Date:	February, 1998

17.

Principle Investigator:	CAD Software Grant
Title:	WorkView Office and ORCA Foundry Design Entry and Synthesis Software
Funding Agency:	Lucent Technologies, Inc., Allentown, PA
Funding Level:	$10,000.00
Date:	September, 1997

18.

Co-Principle Investigator:	Contract No. 461219
Title:	Microcomputer Architecture Implementation in Field Programmable Gate Arrays
Funding Agency:	Battelle Research Triangle Park Office, US Army Research Laboratory, Adelphi, MD
Funding Level:	$22,800.00
Duration:	August 18, 1997-September 30, 1998

19.

Principle Investigator:	Contract No. DAAL03-91-C-0034 US Army Summer Faculty Research and Engineering Program
Title:	Formal Specification and Verification of High-Performance Reactive and Real-Time Systems
Funding Agency:	U.S. Army
Funding Level:	$12,588.00
Duration:	June-August, 1995

20.

Principle Investigator:	Instruction/Research Computer Software Grant (Integrated CAD/CAE Tools)
Title:	An Engineering Workstation Based Integrated Computer Engineering/Science Laboratory
Funding Agency:	Mentor Graphics Corporation
Funding Level:	$732,025.00
Date:	April 1994

21.

Co-Principal Investigator:	Instruction/Research Equipment Grant
Title:	Integrated Computer Engineering Laboratory
Funding Agency:	Kentucky Council On Higher Education
Funding Level:	$10,356.
Date:	February 23, 1993

22.

Principle Investigator:	Research Initiation Grant
Title:	A Homogeneous Computer Architecture Framework and Structure for an Automated Manufacturing Environment
Funding Agency:	UK Center for Robotics and Manufacturing Systems
Funding Level:	$24,969.
Date:	12 Months (July 1, 1990 - June 30, 1991)

23.

Co-Principal Investigator:	Research Equipment Grant
Title:	Digital Education Commitment Grant
Funding Agency:	Digital Equipment Corporation
Funding Level:	$100,000.
Date:	November 14, 1986

24.

Co-Principal Investigator:	Computer Equipment Donation
Title:	STC Computing Equipment Donation
Funding Agency:	Storage Technology Corp. (STC)
Funding Level:	$403,000.
Date:	April 13, 1984

25.

Principal Investigator:	Contract No. DASG60-82-C-0024
Title:	Switching for Data Driven/Flow Computer Architectures.
Funding Agency:	U. S. Army Ballistic Missile Defense Systems Command, Huntsville, AL
Funding Level:	$49,976.
Duration:	12 Months (February 1982 - February 1983)

26.

Co-Principal Investigator:	Major Research Equipment Grant
Title:	Digital Engineering Laboratory Research Equipment
Funding Agency:	University of Kentucky Graduate School
Funding Level:	$11,760.
Date:	November 1980

27.

Principal Investigator:	Contract No. DASG60-80-Q-0174
Title:	A Dynamic Pipeline Computer Architecture for Data Driven Systems
Funding Agency:	U. S. Army Ballistic Missile Defense Systems Command, Huntsville, AL
Funding Level:	$78,056.
Duration:	15 Months(September 1980-December 1981)

28.

Principal Investigator:	Contract No. DASG60-79-C-0052
Title:	A Dynamically Alterable Topology for Distributed Processing
Funding Agency:	U. S. Army Ballistic Missile Defense Systems Command, Huntsville, AL
Funding Level:	$49,687.
Duration:	12 Months (April 1979 - May 1980)

29.

Co-Principal Investigator:	Contract No. NAS10-8354
Title:	Development of Digital Instrumentation for Automatically Determining Contamination Levels in Space Shuttle and Ground Support Dynamic Fluid Systems
Funding Agency:	National Aeronautics and Space Administration, Kennedy Space Center, FL
Funding Level:	$60,000.
Duration:	24 Months (May 1973 - April 1975)

PUBLICATIONS

Books, Book Chapters and Parts of Book Chapters

1. G. Broomell and J. R. Heath, "Circuit Switching Topologies," Part of Chapter 2 in: C. Dhas, V. K. Konangi and M. Sreetharan (Editors), *BROADBAND SWITCHING; Architectures, Protocols, Design and Analysis*, IEEE Computer Society Press Tutorial, Los Alamitos, California, pp. 107-145, 1991.

Refereed Full-Paper Conference Proceedings and Journal Publications

1. James R. Heath, "Reducing Quantizer Deadband with a 'Range-Switching' Digital Filter," *Master's Thesis*, Auburn University, Auburn, AL, January, 1969. (Nominated for Annual Auburn University Chapter of Sigma Xi Research Award of the Year.)

2. James R. Heath , Chester C. Carroll, and H. T. Nagle, "Reducing Quantizer Deadband with a Range-Switching Digital Filter," *Proceedings of the 1969 IEEE Computer Conference*, Minneapolis, MN, pp.78-81, June, 1969.
3. James R. Heath and Chester C. Carroll, "A Variable Range Digital Filter Design," *Proceedings from the Third ASILOMAR Conference on Circuits and Systems*, Pacific Grove, California, pp.269-275, December, 1969.
4. James R. Heath and Chester C. Carroll, "A Gain Switching Real-Time Digital Filter," *Proceedings of the 1970 Southeastern System Symposium*, Gainesville, Fl, pp.1-6, March, 1970.
5. James R. Heath and Chester C. Carroll, "Special-Purpose Computer Organization for Double-Precision Realization of Digital Filters," *IEEE Transactions on Computers*, Vol. C-19, No. 12, pp. 1146-1152, December, 1970.
6. James R. Heath, "Range Adaptive Digital Filtering," *Ph.D. Dissertation*, Auburn University, Auburn, AL, June, 1973.
7. J. R. Heath and H. T. Nagle, Jr., "Design a Floating Point A/D Converter," *Electronic Design*, Vol. 22, No. 11, pp.80-84, May, 1974.
8. J. R. Heath, B. D. Carroll and T. T. Cwik, "An Improved Version of CDL for the Efficient Simulation of Microprocessor and Minicomputer Systems," *Proceedings of the 1977 IEEE Region 3 Conference*, Williamsburg, VA, pp.642-645, April, 1977.
9. J. R. Heath, B. D. Carroll and T. Cwik, "CDL - A Tool for Concurrent Hardware and Software Development?" *Proceedings of the 14th Design Automation Conference*, New Orleans, LA, pp.445-449, June, 1977. (Voted as one of three best papers presented at conference.)
10. J. R. Heath, B. D. Carroll and T. Cwik, "Capabilities and Limitations of CDL as a System Hardware and Software Design Aid - A Summary," *Journal of Design Automation and Fault Tolerant Computing*, (Invited Paper), pp.93-116, May, 1978.
11. W. W. Hatcher and J. R. Heath, "The Development of a High-Level Language and Cross-Compiler for a Microcomputer," *Proceedings of the Eleventh Annual Southeastern Symposium on System Theory*, Clemson University, Clemson, S.C., pp.224-231, March 12-13, 1979
12. J. R. Heath, H. T. Nagle, Jr., and S. G. Shiva, "Realization of Digital Filters Using Input-Scaled Floating Point Arithmetic", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, Vol. ASSP-27, No. 5, pp.469-477, October, 1979
13. E. T. Landrum and J. R. Heath, "Fidelity Optimization of Micro-processor System Simulations,"*Proceedings of the ISMM Eleventh International Symposium on MINI and MICROCOMPUTERS*, Asilomar Conference Grounds, Pacific Grove, California, pp.36-41, January 30-31, February 1, 1980.
14. J. R. Heath, J. Cline and J. Kennedy, "A Dynamically Alterable Topology Distributed Data Processing Computer Architecture," *Proceedings of the IEEE 1980 International Conference on Circuits and Computers*, Port Chester, New York, pp.517-524, October 1-3, 1980
15. J. R. Heath and J. Cline, "The Complexity and Use of Multistage Interconnection Networks for Distributed Processing Systems," *Proceedings of the 1980 IEEE Distributed Data Acquisition, Computing, and Control Symposium*, Miami Beach, Fl, pp.1-8, December 3-5, 1980.

16. J. R. Heath and S. M. Patel, "A Methodology and Example of a Universal, One Pass, Crossassembler for Microprocessors," *Proceedings of IEEE Region 3 SOUTHEASTCON '81*, Huntsville, AL pp.1-8, April 5-8, 1981.
17. J. R. Heath and S. M. Patel, "How to Write a Universal Cross-Assembler," *IEEE MICRO*, Vol. 1, No. 3, pp.45-66, August, 1981
18. A. D. Hurt and J. R. Heath, "A Data Flow Language and Interpreter for a Reconfigurable Distributed Data Processor," *Proceedings of 1982 IEEE International Conference on Circuits and Computers*, New York, NY, pp.56-59, September 29 - October 1, 1982.
19. A. D. Hurt and J. R. Heath, "The Design of a Fault-Tolerant Computing Element for Distributed Data Processors," *Proceedings of the 3rd IEEE International Conference on Distributed Computing Systems*, Miami/Ft. Lauderdale, Florida, pp.171-176, October 18-22, 1982.
20. J. R. Heath, A. D. Hurt, and G. D. Broomell, "A Distributed Computer Architecture for Real-Time, Data Driven Applications," *Proceedings of the 3rd IEEE International Conference on Distributed Computing Systems*, Miami/Ft. Lauderdale, Florida, pp.630-638, October 18-22, 1982.
21. A. D. Hurt and J. R. Heath, "A Hardware Task Scheduling Mechanism for a Real-Time Multimicroprocessor Architecture," *Proceedings 1982 IEEE Real-Time Systems Symposium*, Los Angeles, California, pp.113-123, December 7-9, 1982.
22. G. Broomell and J. R. Heath, "Classification Categories and Historical Development of Circuit Switching Topologies," *ACM Computing Surveys*, Vol. 15, No. 2, pp. 95-133 June 1983.
23. G. Broomell and J. R. Heath, "An Integrated-Circuit Crossbar Switching System Design," *Proceedings of 4th International Conference on Distributed Computing Systems,* San Francisco, California, pp.278-287, May 14-18, 1984.
24. J. R. Heath, "A Note on 'Realization of Digital Filters Using Input-Scaled Floating- Point Arithmetic'," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, Vol. ASSP-34, No. 4, pp. 995, August, 1986.
25. J. R. Heath and E. A. Disch, "A Methodology for the Control and Custom VLSI Implementation of Large Scale Clos Networks," *Proceedings 1988 IEEE International Conference on Computer Design: VLSI In Computers and Processors*, Rye Brook, New York, pp. 472-477, October 3-5, 1988.
26. J. R. Heath, J. Cochran and W. A. Chren, Jr., "A Flow Graph Analysis Algorithm for a Data Driven Reconfigurable Parallel Pipelined Computer Architecture," *Proceedings IEEE Region III Southeastcon'89*, Columbia, South Carolina, pp. 639-644, April 9-12, 1989.
27. J. R. Heath and S. Riley, "Modeling and Implementation of an N x N Clos-Type Interconnect Network Employing a "Clashing" Control Procedure," *Proceedings IEEE Region III Southeastcon'89*, Columbia, South Carolina, pp. 1211-1215, April 9-12, 1989.
28. J. R. Heath and S. Ramamoorthy, "Design and Performance of a Modular Hardware Process Mapper (Scheduler) for a Real-Time Token Controlled Data Driven Multiprocessor Architecture," *Proceedings of the 23rd Southeastern Symposium on System Theory*, Columbia, South Carolina, pp. 478-482, March 10-12, 1991.
29. Tae W. Cho, Sam S. Pyo and J. R. Heath, "A New Conflict Resolving Switchbox Router," *Proceedings of the Second Great Lakes Symposium on VLSI*, Kalamazoo, Michigan, pp. 95-102, February 28-29, 1992.

30. B. Pharmasetiawan, T.S. Chung, J. Fei, and J.R. Heath, "Digital Redesign of Continuous Control System Via Fuzzy Logic Control", *Proceedings of The 32nd IEEE Conference on Decision and Control*, pp. 1282-1283, San Antonia, Texas, Dec. 15-17, 1993.
31. T.W. Cho, S.S. Pyo, and J.R. Heath, "PARALLEX: A Parallel Approach to Switchbox Routing", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 6, pp. 684-693, June, 1994.
32. J. R. Heath, "Published Review of: *Computer Organization and Design: The Hardware/Software Interface* by David A. Patterson and John L. Hennessey, Morgan Kaufmann Publishers, 1994", *COMPUTER*, IEEE Computer Society, pp 118, March, 1995.
33. J.R. Heath, S. Ramamoorthy, C.E. Stroud, and A. Hurt, "Modeling, Design, and Performance Analysis of a Parallel Hybrid Data/Command Driven Architecture System and its Scalable Dynamic Load Balancing Circuit", *IEEE Trans. on Circuits and Systems, II: Analog and Digital Signal Processing*, Vol. 44, No. 1, pp. 22-40, January, 1997.
34. J.R. Heath and B. Sivanesa, "Development, Analysis, and Verification of a Parallel Hybrid Data-flow Computer Architectural Framework and Associated Load Balancing Strategies and Algorithms via Parallel Simulation", *SIMULATION*, Vol. 69, No. 1, pp. 7-25, July, 1997.
35. G. Westerman, J.R. Heath, and C. Stroud, "Delay Fault Testablility Modeling with Temporal Logic", *1997 IEEE AUTOTESTCON Proceedings*, Anaheim, CA, pp.376- 382, Sept., 1997.
36. G. Westerman, R. Kumar, C. Stroud, and J. R. Heath, "Discrete Event System Approach for Delay Fault Analysis in Digital Circuits", *Proceedings 1998 American Control Conference*, Philadelphia, PA, pp.239-243, June 24-26, 1998.
37. G. Westerman, C. Stroud, J. R. Heath, and R. Kumar, "Delay Fault Analysis Using Discrete Event System Approach", *1998 IEEE AUTOTESTCON PROCEEDINGS*, Salt Lake City, UT, pp.22-27, Aug. 24-27, 1998.
38. J. R. Heath, W. D. Leong, C. Stroud, and T. R. Damarla, "Procedures for the Development of Legacy Processor Systems and a Procedure Verifying Case-Study Example", *Proceedings of the 12th Annual IEEE International ASIC/SOC Conference*,Washington, DC, pp. 181-185, Sept. 15-18, 1999.
39. J. R. Heath, C. E. Stroud, and W. D. Leong, "Development of a Test Environment for Pre- and Post-Synthesis Verification of Correct VHDL Description of Core Processor Systems", *Proceedings of the VHDL International Users Forum (VIUF) Fall Workshop '99"*, Orlando, FL, pp. 40-46, Oct. 4-6, 1999.
40. A. V. Radun, J. R. Heath, and K. K. Hon, "Implementation and Verification of the Feedback Control Software Function of a Switched Reluctance Cycloconverter Controller", *Proceedings of the 25th Annual Conference of the IEEE Industrial Electronics Society*, San Jose, CA, 6 pps, Nov. 29-Dec. 3, 1999.
41. Nick J. Vocke, Charles E. Stroud, J. Robert Heath, William R. Orso, and Khushru S. Chhor., "Computer Aided Routing for Complex Programmable Logic Device Manufacturing Test Development", *Proceedings of IEEE SoutheastCon'2000 Conference*, Nashville, TN, 8 pps., April 7-9, 2000.
42. J.R. Heath, A.V. Radun, and K.K. Hon, "Development, Application, and Verification of a Digital Model of the 3-Phase Current Regulator Function of a Switched Reluctance Cycloconverter Controller", *Proceedings of the 2000 IEEE International Conference on Control Applications*, Anchorage, Alaska, 6 pps., Sept. 25-27, 2000.

43. J.R. Heath and S. Durbha, "Methodology for Synthesis, Testing, and Verification of Pipelined Architecture Processors from Behavioral-Level-Only HDL Code and A Case Study Example", *Proceedings of the 2001 IEEE SoutheastCon Conference*, Clemson, South Carolina, 7 pps., Mar. 30-Apr. 1, 2001.
44. J.R. Heath and A. Tan, "Modeling, Design, Virtual and Physical Prototyping, Testing, and Verification of a Multifunctional Processor Queue for a Single-Chip Multiprocessor Architecture", *Proceedings of 2001 IEEE International Workshop on Rapid Systems Prototyping*, Monterey, California, 6 pps. June 25-27, 2001.
45. J.R. Heath, N. J. Vocke, C. E. Stroud and J. Emmert, "Routing Algorithms for Programmable Logic Device Design and Manufacturing Test Development", *Proceedings of the 2001 IEEE AUTOTESTCON Conference*, Valley Forge, Pennsylvania, 15 pps. August 20-23, 2001.
46. J. Robert Heath and Sreenivas Durbha, "A Methodology for and Experiences with Behavioral-Level-Only HDL Code Capture, FPGA Prototype Synthesis, and Verification of Correct Synthesis of a Pipelined Architecture Processor", *Proceedings of the International HDL Conference and Exhibition*, San Jose, CA, 8 pps, March 11-12, 2002.
47. T. F. Burks, S. A. Shearer, J. D. Green, and J. R. Heath, "Influence of Weed Maturity Levels on Species Classification Using Machine Vision", *Journal of Weed Science*, Vol. 50(6), pp. 802-811, 2002.
48. A. T. Wong, J. R. Heath, and M. Lhamon, "A New Scalable Systolic Array Processor Architecture for Simultaneous Discrete Convolution of k Different (n x n) Filter Coefficient Planes with a Single Image Plane", *Proceedings of the 2003 IS&T/SPIE Symposium on Electronic Imaging Science and Technology*, Santa Clara, CA, 12 pps, January 20-24, 2003.
49. Xiaohui Zhao, J. Robert Heath, Paul Maxwell, Andrew Tan, and Chameera Fernando, "Development and First-Phase Experimental Prototype Validation of a Single-Chip Hybrid and Reconfigurable Multiprocessor Signal Processor System", *Proceedings of the 2004 IEEE Southeastern Symposium on System Theory*, Atlanta, GA, 5pps, March 14-16, 2004.
50. M. Muthulakshmi, J. Robert Heath, Kenneth L. Calvert, and James Griffioen, "ESP: A Flexible, High-Performance, PLD-Based Network Service", *Proceedings of the 2004 IEEE International Conference on Communications*, Paris, FRANCE, 5 pps, June 20-24, 2004.
51. Albert T. Wong, J. Robert Heath and Michael Lhamon, "At Last! – A New Ultimately Flexible Discrete Convolution Architecture (Maybe!!): Its Design and Validation", *Proceedings of the 2005 Design and Verification Conference*, San Jose, CA, 9 pps, February 14-16, 2005.
52. Venugopal Duvvuri, J. Robert Heath, Kanchan Bhide and Sridhar Hegde, "A New Processor-to-Memory Crossbar Interconnect Network with a Variable Priority Memory Contention Resolution Protocol for Multiprocessor Architectures", *Proceedings of the 2005 International Conference on Information Systems: New Generations*, Las Vegas, NV, 6pps, April 4-6, 2005.
53. M. Muthulakshmi, J. Robert Heath, Kenneth L. Calvert and James Griffioen, "A Node-Processor Microarchitecture for Implementation of the ESP Network Service Development Paradigm", *Proceedings of the 2005 International Conference on Information Systems: New Generations*, Las Vegas, NV, 6pps, April 4-6, 2005.

54. J. Robert Heath, Sridhar Hegde, Kanchan Bhide, Paul Maxwell, Xiaohui Zhao and Venugopal Duvvuri, "Design, Development and Validation Testing of a Versatile PLD Implementable Single-Chip Heterogeneous, Hybrid and Reconfigurable Multiprocessor Architecture", *Proceedings of the 8th Military and Aerospace Programmable Logic Devices (MAPLD) International Conference*, Washington, DC, 8pps, September 7-9, 2005.
55. T.F. Burks, S.A. Shearer, J.R. Heath and K.D. Donohue, "Evaluation of Neural Network Classifiers for Weed Species Discrimination", *BioSystems Engineering*, Vol. 91(3), pp. 293-304, 2005.
56. Kalyan Phani Tangirala, J. Robert Heath, Arthur Radun and Terry Conners, "Development and Validation of a Programmable Logic Device (PLD) Based Sensor and Processor Microarchitecture System for Equilibrium Moisture Content Calculation in Wood Industries", *Proceedings of the 2006 IEEE Sensors and Applications Symposium*, Houston, TX, 6 pps, February 7-9, 2006.
57. Chunfang Zheng and J. Robert Heath, "Simulation and Visualization of Resource Allocation, Control, and Load Balancing Procedures for a Multiprocessor Architecture", *Proceedings of the 17th International Association of Science and Technology for Development (IASTED) International Conference on MODELING AND SIMULATION*, Montreal, Canada, 6pps, May 24-26, 2006.
58. A. T. Wong, J. R. Heath, and M. Lhamon, "A New Systolic Array Processor Architecture for Simultaneous Discrete Convolution of an Image Plane with Multiple Filter Coefficient Sets", *SPIE Journal of Electronic Imaging*, Vol. 16, No. 1, 12 jps, January-March, 2007.
59. Srilaxmi Pampana, J. Robert Heath and Arthur V. Radun, "Modeling and FPGA Based Implementation of a Position Estimator for Control of Switched Reluctance Motors", *Proceedings of the 5th IASTED International Conference on Circuits, Signals and Systems*, Banff, Alberta, Canada, 6pps, July 2-4, 2007.
60. Ruigang Yang, Subhasri Krishnan and J. Robert Heath, "Flexible Pixel Compositor for Autostereoscopic Displays", *Proceedings of the 2008 IS&T/SPIE Conference on Stereoscopic Displays and Applications XIX*, San Jose, CA, 12 pps, January 27-31, 2008.
61. Phani Tangirala, J. Robert Heath, Arthur Radun and Terry Conners, "A Hand-Held Programmable-Logic-Device Based Temperature and Relative-Humidity Sensor, Processor and Display System Platform for Automation and Control of Industry Processes", *Proceedings of the 2008 IEEE Industry Applications Society Annual Meeting*, Edmonton, Alberta, Canada, 8 pps, October 5-9, 2008.
62. V. Bhargav Alluri, J. Robert Heath and Michael Lhamon, "A Multi-Channel Coherent Amplitude Modulated Time Division Multiplexed Software Defined Radio Receiver Architecture for Programmable-Logic-Device Technology Implementation", *Proceedings 2009 IEEE MTT-S Radio and Wireless Symposium*, San Diego, CA, 4 pps, January 18-22, 2009.
63. J. Robert Heath, Nien Yi Lim, Kenneth L. Calvert and James Griffioen, "A New Reconfigurable Network Node Processor Architecture for Distributed Implementation of Ephemeral State Processing", *Proceedings of the 22nd ISCA International Conference on Parallel and Distributed Computing and Communications Systems*, Louisville, KY, 8 pps, Sept. 24-26, 2009.

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65. Phani Tangirala, J. Robert Heath, Arthur Radun and Terrance E. Conners, “A Hand-Held Programmable-Logic-Device Based Temperature and Relative-Humidity Sensor, Processor and Display System Platform for Automation and Control of Industry Processes”, *IEEE Transactions on Industry Applications,* Vol. 46, No. 4, 11 jps, July/August, 2010.
66. V. Bhargav Alluri, J. Robert Heath and Michael Lhamon, “A New Multi-Channel, Coherent Amplitude Modulated, Time Division Multiplexed, Software Defined Radio Receiver Architecture and Field-Programmable-Gate-Array Technology Implementation”, *IEEE Transactions on Signal Processing,* Vol. 58, No. 10, 16 jps, Oct. 2010.
67. Rishvanth K. Venugopal, J. Robert Heath and Daniel L. Lau, “FPGA Based Parallel Architecture Implementation of Stacked Error Diffusion Algorithm”, *Proceedings of the 2011 IEEE Symposium on Application-Specific Processors,* San Diego, CA, 4pps, June 5-6, 2011.

Papers in Review or To Be Submitted

1. J. R. Heath, M. Qiu, S. Hegde, and K. Bhide, “Development and Validation of a Heterogeneous Reconfigurable CMP”, (To be submitted for journal review).
2. J. R. Heath and A. Tan, “Modeling, Organization, Architecture, Development, and Hardware Prototype Testing and Validation of a Multifunctional Processor Queue Component”, (To be submitted for journal review).

Technical and Research Reports

1. Chester C. Carroll, J. R. Heath, et. al., "Reducing Quantizer Deadband with a Range-Switching Digital Filter," Fifteenth Technical Report, NAS8-11274, Auburn Research Foundation, Auburn, Alabama, February, 1969.
2. Chester C. Carroll, J. R. Heath, et. al., "Digital Filter Specifications," TR #12, NAS8-20163, Auburn Research Foundation, Auburn, Alabama, February, 1970.
3. J. R. Heath, "Design of Interface Electronics for a Special Laser Designator Unit," Final Report, Contract Number DO 0579, Battelle, Columbus Laboratories, Durham Operations, Durham, North Carolina, August, 1977.
4. J. R. Heath, "Feasibility of a Distributed Computer System for the National Tillage Machinery Laboratory," Final Report, National Tillage Machinery Laboratory, United States Department of Agriculture, Auburn, Alabama, September, 1977.
5. J. R. Heath, "Recommendations Towards the Selection of a Specific Distributed (Networked) Computer Systems for the National Tillage Machinery Laboratory, U. S. Department of Agriculture, Auburn, Alabama, September, 1978.
6. J. R. Heath, "An Algorithm for Plotting Laser Spot Energy Contour Maps and Recommendations for More Efficient Computer Evaluation of Video and Laser Target Tracking Systems," Final Report, DO#0910, Army Research Office, Scientific Services Program, Battelle Columbus Laboratories, Durham, North Carolina, November 14, 1978.

7. J. R. Heath, et. al., "A Dynamically Alterable Topology for Distributed Processing: Final Report," Contract No. DASG60-79-C-0052, University of Kentucky Research Foundation, Lexington, Kentucky, June, 1980.
8. J. R. Heath, et. al., *Addendum to: A Dynamically Alterable Topology for Distributed Processing: Final Report,* Contract No. DASG60-79-C-0052, Department of Electrical Engineering, University of Kentucky, Lexington, Kentucky, February, 1981.
9. J. R. Heath, et. al., "A Dynamic Pipeline Computer Architecture for Data Driven Systems: Final Report," Contract No. DASG60-79-C-0052, University of Kentucky Research Foundation, Lexington, Kentucky, February, 1982.
10. J. R. Heath, et. al., "Switching for Data Drive/Flow Computer Architectures: Final Report," Contract No. DASG60-82-C-0024, University of Kentucky Research Foundation, Lexington, Kentucky, April, 1983.
11. J. R. Heath, et. al., *University of Kentucky Six-Year Computing Plan*, University of Kentucky, Lexington, Kentucky, September, 1983.
12. J. R. Heath, et. al., *University of Kentucky Five-Year Plan for Computing and Information Systems: 1985-1990*, University of Kentucky, Lexington, Kentucky, October, 1985.
13. J. R. Heath, "Overview of Methods for Cost Justifying Computer Integrated Manufacturing (CIM)," Square D Corporation, Lexington, Kentucky, August, 1990.
14. J. R. Heath and Fan Hu, "A Homogeneous Computer Architecture and Structure for an Automated Manufacturing Environment: Final Report," UK Center for Robotics and Manufacturing Systems, University of Kentucky, Lexington, Kentucky, October, 1991.
15. J.R. Heath, "Potential of Temporal Logic for Modeling Real-Time Digital Systems" Final Report, U.S. Army Research Office, P.O. Box 12211, Research Triangle Park, NC 27709, Contract No. DAAL03-91-C-0034, Oct. 1995.
16. J. R. Heath and C. Stroud, "Microcomputer Architecture Implementation in Field Programmable Gate Arrays", *Final Report: Contract No. 461219,* Army Research Laboratory, Adelphi, MD, October, 1998
17. Albert Tung-Hoe Wong and J. Robert Heath, “A New Scalable Systolic Array Processor Architecture for Discrete Convolution”, *Final Report: Contract No. 5-37947*, Lexmark International, Inc., Lexington, KY, May, 2003.
18. Veerendra Bhargav Alluri and J. Robert Heath, “Multiple Channel Coherent Amplitude Modulated Time Division Multiplexed Software Defined Radio Receiver”, *Contract Task Report: Contract/Account No. 3046947100*, Lexmark International, Inc., Lexington, KY, January, 2008.
19. Pallavi Khandelwal and J. Robert Heath, “Systematic Approach Towards System On Chip Simulation Based Functional Verification”, *Contract Task Report: Contract/Account No. 3046947100,* Lexmark International, Inc., Lexington, KY, July, 2010.

THESIS AND MASTERS PROJECT DIRECTION

Ph.D. Thesis Direction

1. Tae Won Cho, "PARALLEX: A Parallel Approach to Switchbox Routing", March, 1992
2. Mohammad Rahmati, "Intensity and Distortion-Invariant Object Recognition and Complex Linear Morphology," December, 1993 (Co-Director with Dr. Laurence Hassebrook)

3. Charles T. Wolfe, “A Parallel Finite Element Algorithm for the Solution of the Helmholtz Wave Equation”, May, 2007 (Co-Director with Dr. Stephen Gedney)

Masters Thesis Direction

1. John Houston McElreath, "On the use of Microcomputers as Terminals on a Minicomputer Based Timeshare System", August, 1976
2. Robert P. Dean, "An Interface and Application of a Magnetic Tape Unit", December, 1976
3. Shailesh M. Patel, "An Adaptable One Pass Cross Assembler for Microprocessors", December, 1977
4. William W. Hatcher, "Development of a High Level Language and Cross - Compiler for the Intel 8080 Microprocessor", June, 1979
5. Richard L. Stewart, "Considerations for an Assembler Scheduled Multi-Microprocessor System", August, 1980
6. James D. Kennedy, "The Hardware Design of a Dynamically Alterable Topology Distributed Data Processing System", 1980
7. Earnest Taylor Landrum, Jr., "Fidelity Optimization of Microprocessor System Simulations", December, 1980
8. Eric a Disch, "A Methodology for the Control and Implementation of Large-Scale Clos Networks", 1981
9. Andrew D. Hurt, "The Design of a Distributed, Fault Tolerant, Dynamic Pipeline Computer Architecture and Its Distributed Fault-Tolerant Operating System", 1981
10. James H. Cline, "Modeling and Design of Interconnection Networks for Distributed Data Processing Systems", 1981
11. James D. Cochran, "Mathematical Modeling and Analysis of a Dynamic Pipeline Computer Architecture, 1982
12. Hiten D. Varia, "Simulation of a Dynamically Reconfigurable Macropipline Computer System", 1982
13. Nhan D. Tran, "A Universal Cross Assembler for Microprocessors", October, 1982
14. Maturi S. Rao, "A Graphic Simulation of a Dynamic Pipeline Computer Architecture", 1983
15. Ronald W. Wilder, "Real Time Simulator for Numerical Integration Solution of Differential Equiations with Analog Inputs and Outputs", 1984
16. William D. Walburg, "Mapping Processes to Computing Elements for a Data Flow Computer", August, 1990
17. Balasubramanian Sivanesa, "Dynamic Resource Allocation in a Data-Driven Reconfigurable Parallel-Pipelined Computer Architecture", August, 1995.
18. Kah Kee Hon, "Hardware Implementation of Switched Reluctance Cycloconverter System Controller", December, 1998.
19. Weng Dean Leong, "Re-engineering, Synthesis, and Testing of Legacy Computer Systems", December, 1998.
20. Sreenivas Durbha, "Prototyping and Testing of a Pipelined Processor from Behavorial Level HDL Code", December, 1999.
21. Andrew Tan, "Modeling, Development and Testing of a Multifunctional Processor Queue", May, 2000.

22. Nick J. Vocke, "Computer Aided Routing Algorithm Development for Complex Programmable Logic Device Test Development", July, 2000 (Co-Directed with Dr. Charles Stroud).
23. Albert Tung-Hoe Wong, “A New Scalable Systolic Array Processor Architecture for Discrete Convolution”, May, 2003.
24. M. Muthulakshmi, “Processor Microarchitecture for Implementation of Ephemeral State Processing Within Network Routers”, August, 2003.
25. Srilaxmi Pampana, “FPGA Based Implementation of a Position Estimator for Controlling a Switched Reluctance Motor”, Dec. 2004 (Co-Directed with Dr. Arthur Radun).
26. Chunfang Zheng, “Graphical Modeling and Simulation of a Hybrid Heterogeneous and Dynamic Single-Chip Multiprocessor Architecture”, Dec. 2004.
27. Kanchan P. Bhide, “Design Enhancement and Integration of a Processor-Memory Interconnect Network into a Single-Chip Multiprocessor Architecture”, Dec. 2004.
28. Sridhar Hegde, “Functional Enhancement and Applications Development for a Hybrid, Heterogeneous Single-Chip Multiprocessor Architecture”, Dec. 2004.
29. Kalyan Phani Tangirala, “Development and Validation of a Special Purpose Sensor and Processor System to Calculate Equilibrium Moisture Content of Wood”, May, 2005 (Co-Directed with Dr. Arthur Radun).
30. Dragomir Milisav Nikolic, “An Improved Method and Apparatus for Automated Design and Verification of Integrated Circuits”, December 2005.
31. Subhasri Krishnan, “A Control Algorithm to the Anywhere Pixel Router”, August, 2007 (Co-Directed with Dr. Ruigang Yang).
32. Veerendra Bhargav Alluri, “Multiple Channel Coherent Amplitude Modulated Time Division Multiplexed Software Defined Radio Receiver”, December, 2007.
33. Robert Muyskens, “Design and Validation of a Virtual Printhead Architecture for Testing of an Inkjet Printhead Apparatus”, August, 2008.
34. Rishvanth Kora Venugopal, “FPGA Based Parallel Architecture Implementation of Stacked Error Diffusion Algorithm”, December, 2010.

Masters Project Direction

1. David W. Glass, "An Overview of Optical Computing", April, 1989.
2. Saivenkatesh Ramamoorthy, "Hardware and Software Process Mapping Mechanisms for a Parallel Data Driven Architecture and a Performance Comparison", August, 1989.
3. Venktesh S. Maudgalya, " An Overview of Dataflow Computers", 1990.
4. U. Chameera R. Fernando, "Modeling, Design, Prototype Synthesis and Experimental Testing of a Dynamic Load Balancing Circuit for a Parallel Hybrid Data/Command Driven Architecture", December, 1999.
5. Paul Maxwell, "Design Enhancement, Synthesis, and Field Programmable Gate Array Post-Implementation Simulation Verification of a Hybrid Data/Command Driven Architecture", May, 2001.
6. Venugopal Duvvuri, “Design, Development, and Simulation/Experimental Validation of a Crossbar Interconnect Network for a Single-Chip Shared Memory Multiprocessor Architecture”, June, 2002.

7. Xiaohui Zhao, “Hardware Description Language Simulation and Experimental Hardware Prototype Validation of a First-Phase Prototype of a Hybrid Data/Command Driven Multiprocessor Architecture”, May, 2002.
8. Guru Vamshi Krishna Vankadara, “SystemVerilog and It’s Potential for Concise Digital System Design Documentation/Description and Faster Design Validation and/or Verification”, May, 2009.
9. Pallavi Khandelwal, “Systematic Approach Towards System On Chip Simulation Based Functional Verification”, May, 2010.
10. Zachary Fister, “Coverage Driven Constrained Random Test Parameter Selection”, May, 2011.

CONSULTING ACTIVITIES

Battelle, Research Triangle Park, NC
Square D. Corporation, Lexington, KY
U. S. Army Missile Command, Redstone Arsenal, Huntsville, AL
National Tillage Machinery Laboratory, USDA, Auburn, AL
Advanced Technology Institute, Auburn, AL

PRESENTATIONS

Seminars on Information Systems Planning and Policy Development.
Computer Engineering Seminars at Universities and Federal Research Laboratories.
Most Conference Papers Listed Under PUBLICATIONS Section.

UNIVERSITY SERVICE

Member, Fayette County Public School Task Force on Development of A Strategic Plan For Excellence In Education
Advisor to Fayette County Public Schools on Computing Technology Issues
Teaching of University Sponsored Shortcourses Related to Computing
Instructor for UK101 - A Course Which Acclimates Freshman Students to University Life
Instructor in Summer Gifted Students (Ages 12-18) Program (University of Kentucky)
Co-operative Education Coordinator for the Electrical Engineering Department
University Patent Committee
University Research Advisory Committee
Many Other Departmental, College, and University Ad-hoc Committees.
University Faculty Senate Member from Engineering
University Graduate Council Member from Engineering
Faculty Advisor to Eta Kappa Nu Student Chapter

ADMINISTRATIVE EXPERIENCE

1. **Position:** Associate Vice President for Information Systems Planning and Policy and Director of the Computing Center, University of Kentucky (1982-1987).

Job Function Overview

Reporting to the offices of the Vice President for Administration of the University of Kentucky and the Vice-Chancellor of Academic Affairs of the Lexington Campus of the University of Kentucky, the position included executive responsibility for University-wide Academic and Administrative Information Systems Planning and Policy Development, Budgeting, Coordination and Implementation, and direct management responsibility for the University Computing Center and Data Communication Network Systems. The University consisted of Central Administration, a Main Lexington Campus, a Medical Center, a 13 college Community College System; all with a total enrollment of approximately 50,000 students, 2200 faculty, 7100 staff and a $500,000,000. annual operating budget. The combined Academic and Administrative Computing Center and Data Communication Network Systems was staffed with approximately 80 FTE permanent staff and approximately 20-30 part time student employees

Accomplishments

Development and implementation of First and Second formal University-wide Five-Year Computing and Information Systems Plans. Implementation of plans moved the University from a mostly mainframe batch environment with no data communications networks to a networked and distributed three tiered hierarchial environment allowing interactive and batch and personal computing. The resulting hardware environment consisted of a supercomputer, mainframes, and distributed minicomputers and personal computers interfaced where needed through a Campus data communications network. A rich complement of academic software and administrative systems were added and implemented during the time period.